REMARKS

Applicants respectfully request reconsideration of this application as amended. Claims 1-3, 8, 10, 11, 12, 18, 22-24, 28, and 29 have been amended. No claims have been canceled. Therefore, claims 1-29 are now presented for examination.

In a Final Office Action, filed April 22, 2004, claims 1-29 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the Examiner asserts that the term "data access primitive" is indefinite. Applicants submit that the rejection has been obviated since claims 1-3, 8, 10, 11, 12, 18, 22-24, 28, and 29 have been amended to replace the term.

Claim 1, 18, and 24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Dangelo (U.S. Patent No.6,324,678) in view of Tabak. Applicant submits that the present claims are patentable over Dangelo in view of Tabak.

Dangelo discloses an electronic CAD system operated with a suite of software tools for enabling a designer to create and validate a structural description and physical implementation of a device from a behavior-oriented description using a high-level computer language. First, a designer specifies the desired behavior of the device in a high-level language, such as VHDL. The description includes high-level timing goals. Next, the designer iterates through simulation and design changes until the desired behavior is obtained. Next, the design is partitioned into a number of architectural blocks by exploring the "design space" of architectural choices, which can implement the design behavior. Next, in a "logic synthesis" step, a number of separate programs are used to efficiently synthesize the different architectural blocks identified in the partitioning step. Those blocks having highly regular structures or well understood functions are directed to specific synthesis tools (e.g. memory or function compilers). Those blocks with random or unstructured logic are directed to more

general logic synthesis programs. The output of this step is a net list of the design. Next, in a "physical simulation" step, the gate-level design description is simulated, comparing the results with those from the initial behavioral simulation. Finally the design is input to existing software systems that control the physical implementation of the design, such as in an ASIC (Application Specific Integrated Circuit) device. See Dangelo at col. 3, ll. 35 - col. 4, ll. 28.

However, Dangelo does not disclose or suggest replacing the logic design component with logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections for the memory-mapped device based upon the logic design component and the first starting address.

In fact, the Examiner has admitted in the Office Action that Dangelo does not disclose an addressing matching function, lane matching function and one or more bus connections for the memory-mapped device based upon the logic design component and the first starting address. See Final Office Action at page 6, paragraphs 39 and 40, and page 7, paragraphs 42-44.

Tabak discloses various microprocessor architectures. Tabak further discloses address mapping, which is the mapping between main memory and a cache. The mapping operates in a manner such that, line 0 from main memory is stored in set 0 in the cache, line 1 in set 1 and so forth until the number of sets in the cache are exhausted. Then the count starts again with set 0. See Tabak at pg. 48, ll. 21-22.

Claim 1 of the present application recites replacing a logic design component with logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections for a memory-mapped device based upon the logic design component and the first starting address. Applicant submits that the address mapping function disclosed in Tabak is not equivalent to address matching disclosed in applicant's specification and recited in claim 1.

Even if Tabak disclosed using an address matching function, which applicant submits is not the case, Tabak still does not disclose or suggest replacing a logic design component with logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections for the memory-mapped device based upon the logic design component and the first starting address. Using an address matching function in a microprocessor is not the same as replacing a logic design component with logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections.

Similarly, since Dangelo and Tabak do not disclose or suggest replacing the logic design component with logic components that implement a first set of addressing matching function, any combination of Dangelo and Tabak would also not disclose or suggest such a feature. Accordingly, claim 1 is patentable over Dangelo in view of Tabak.

Claims 2-9 depend from claim 1 and include additional features. Thus, claims 2-9 are also patentable over Dangelo in view of Tabak.

Claim 10 recites using a logic design component to specify addressability for a memory-mapped device, addressability comprising an address matching function, a lane matching function and one or more bus connections. Thus, for the reasons described above with respect to claim 1, claim 10 is also patentable over Dangelo in view of Tabak. Since claims 11-17 depend from claim 10 and include additional features, claims 11-17 are also patentable over Dangelo in view of Tabak.

Claim 18 recites selecting a logic design component to provide data access of a desired transaction size, and to indicate an addressing matching function, a lane matching function and one or more bus connections for a memory-mapped device. Thus, for the reasons described above with respect to claim 1, claim 18 is also patentable over Dangelo in view of Tabak. Since claims 19-23 depend from claim 18 and include additional features, claims 19-23 are also patentable over

Dangelo in view of Tabak.

Claim 24 recites selecting a logic design component to provide data access of a desired transaction size, and to indicate an addressing matching function, a lane matching function and one or more bus connections for a memory-mapped device. Thus, for the reasons described above with respect to claim 1, claim 24 is also patentable over Dangelo in view of Tabak. Since claims 25-29 depend from claim 24 and include additional features, claims 25-29 are also patentable over Dangelo in view of Tabak.

Claims 2-17, 19-23, and 25-29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Dangelo (U.S. Patent No.6,324,678) in view of Tabak and Applicant's Admission and MPEP 2144.04 (Routine Expedient of making automatic). Applicant submits that the present claims are patentable over Dangelo and Tabak even in view of background pf the application.

Applicant's background discloses specifying the addressability and bus connections, and the tediousness of a designer to explicitly specify designing for 8-bit and 32-bit system busses. See Specification at pages 1 and 2. However, if anything, applicant's background teaches away from the claims since the claims recite generating first logic components that implement an address matching function, and generating second logic components that implement lane matching function and one or more bus connections.

As described above, neither Dangelo nor Tabak disclose or suggest replacing a logic design component with logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections for the memory-mapped device based upon the logic design component and the first starting address. Therefore, the present claims are patentable over any combination of Dangelo, Tabak and applicant's background since none of the above disclose or suggest replacing a logic design component with logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections for the

memory-mapped device based upon the logic design component and the first starting address.

Applicants respectfully submit that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on June 22, 2004.

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Signature